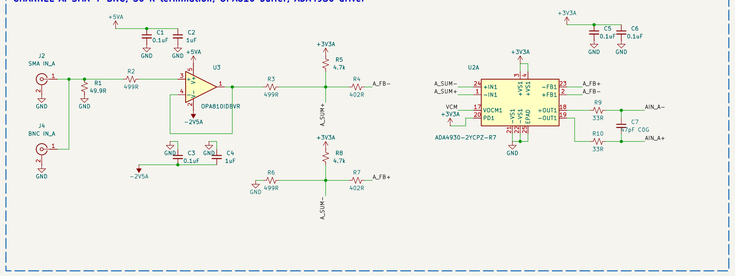
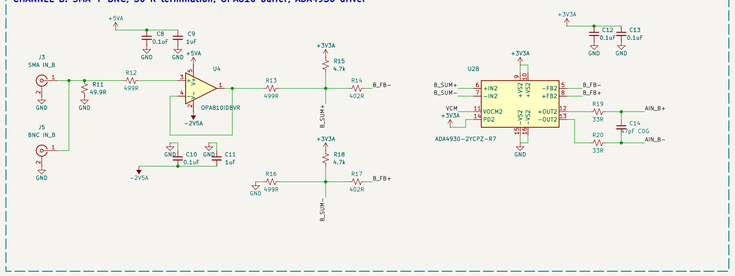
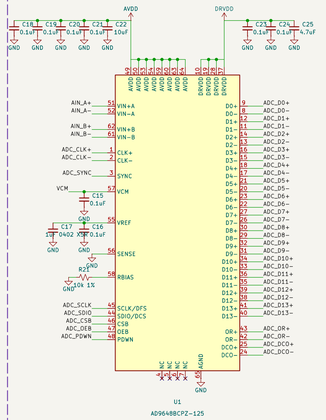
CHANNEL A: SMA + BNC, 50 R termination, OPA810 buffer, ADA4930 driver



CHANNEL B: SMA + BNC, 50 R termination, OPA810 buffer, ADA4930 driver



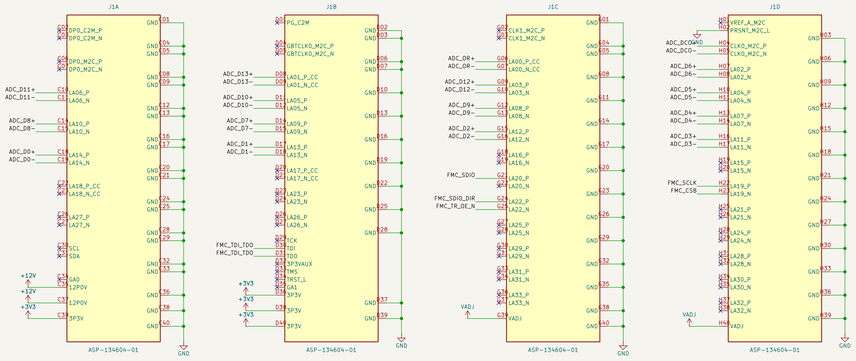
ADC: AD9648 (interleaved LVDS), reference, bias



SENSE = AGND: internal 1.0 V reference, 2 Vpp span.

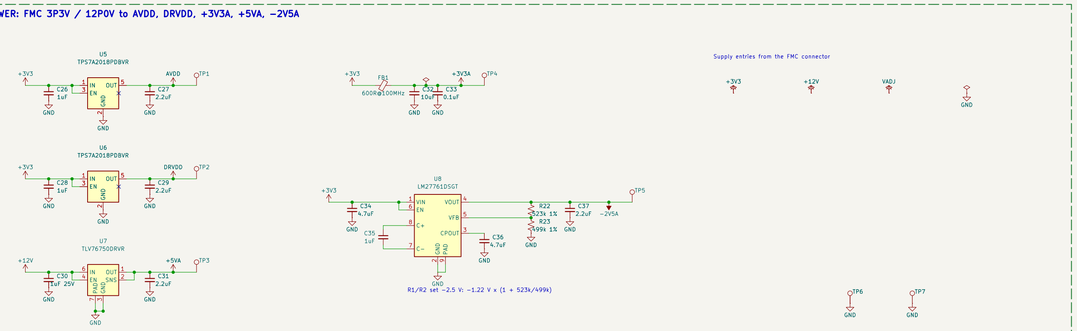
RBIAS 10k 1% per Rev C; NC pins 4–7 left open.

FMC LPC (Samtec ASP-134604-01) to Nexys Video

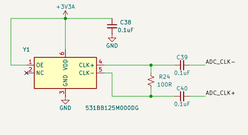


TDI tied to TDO: mezzanine adds no JTAG device. No IPMI EEPROM fitted (SCL/SDA/GA NC); confirm the Nexys Video does not require one.

POWER: FMC 3P3V / 12P0V to AVDD, DRVDD, +3V3A, +5VA, −2V5A

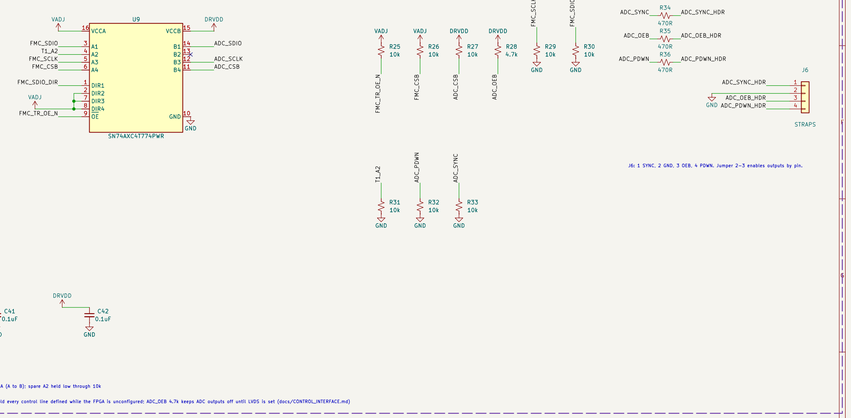


CLOCK: SI531 125 MHz LVDS XO, AC-coupled to ADC CLK



100R termination and series 0.1 uF per AD9648 Fig. 55; ADC CLK inputs self-biased.

CONTROL: SN74AXC4T774 2.5 V (VADJ) <-> 1.8 V (DRVDD), safe defaults



DIR2–4 tied to VCCA (A to B): spare A2 held low through 10k

Pull-ups/downs hold every control line defined while the FPGA is unconfigured: ADC_OEB 4.7k keeps ADC outputs off until LVDS is set (docs/CONTROL_INTERFACE.md)

J6: 1 SYNC, 2 GND, 3 OEB, 4 PDWN. Jumper 2–3 enables outputs by pin.

Sheet: /
File: current_measurement.kicad_sch

Title: Current measurement C3: 2-ch AD9648 FMC mezzanine

Size: A1 Date: Rev:
KiCad E.D.A. 10.0.7 Id: 1/1